REMARKS

Examiner F. Erdem is thanked for the thorough examination and search of the subject Patent Application. Claims 1-16, 19, 20, 24, 28 and 25 are canceled.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of Claims 17, 18, 21-23, 26, and 27 rejected under 35 U.S.C. 102(e) as being anticipated by Zhou et al 6,156,598 is requested based on the following remarks.

Applicant agrees that Zhou et al teaches a method to form a MOSFET device. However, Applicant respectfully submits that Zhou et al does not include a feature of Applicant's claimed invention. In particular, each independent claim (Claims 17, 22, and 26) contains a feature of a liner oxide covering the top of the polysilicon trace as is shown, for example, in lines 10 and 11 of Claim 17 below:

17. (Previously Presented) A MOSFET device comprising:

a gate comprising a polysilicon trace overlying a semiconductor substrate with an insulator therebetween;

a source region and a drain region in said semiconductor substrate with said polysilicon trace laterally between said source and drain regions;

a liner oxide layer overlying said polysilicon trace wherein said liner oxide layer covers sidewalls of said polysilicon trace at said source and drain regions and wherein said liner oxide layer covers the top of said polysilicon trace; and

silicon nitride spacers wherein said liner oxide layer is laterally between said silicon nitride spacers and said polysilicon trace at said source and drain regions and wherein said silicon nitride spacer has an L-shaped profile.

As the Examiner has indicated, the above-described feature is not actually shown in Zhou et al. However, Applicant disagrees that Zhou et al teaches the presence of a liner oxide overlying the polysilicon trace as is taught in Applicant's invention on the following grounds. First, Zhou et al indicates that a liner oxide layer 30 may be formed on the gate structure 20. However, since the liner oxide layer 30 is not shown in any of the drawings, it is indefinite as to where this layer 30 is actually formed. Applicant cannot determine if this liner oxide layer 30 is formed on the top surface of the gate structure 20,

on the sidewalls, under the gate structure 20, or some combination thereof. It is not, therefore, reasonable to use the teachings of the formation of the liner oxide layer 30 as prima facia proof of anticipation of Applicant's claimed invention since this teaching of Zhou et al is indefinite.

Further, Applicant observes that Zhou et al indicates that the liner oxide layer 30, if used, may be employed as an etch stop for the dielectric spacer etch (col. 4, line 28-30). However, this observation does prove that the liner oxide layer 30 remains overlying the gate structure 40 for several reasons. First, since the liner oxide layer 30 is never shown, it is not at all clear that the liner oxide layer 30 is ever overlying the gate structure 20 as indicated above. Second, there are many examples of etch stop layers where the etching material is partially or completely consumed during an etching process for which it is employed as the stopping indicator. Therefore, the optional application of the liner oxide layer 30 as an etch stop is, again, not prima facia proof of the presence of the liner oxide layer 20 overlying the gate structure 30, post etching of the spacers.

The above observations are consistent with the references to the liner oxide layer in column 2, lines 40-41 and lines 49-

50. These references are in a summary section and add no further definitiveness to the location of the liner oxide layer, which is only described as 'on' but not specified as on the top surface, or to the final disposition of the liner oxide layer, which is described as potentially acting as an etch stop layer without indicating if the liner layer remains (or ever is) over the top surface of the gate structure, post etching. Further, these observations regarding the summary section are completely consistent with the references in the Abstract since the text in the summary and in the Abstract is identical.

In summary, Applicant respectfully submits that Zhou et al cannot be used to prove anticipation of Applicant's claimed invention, as recited in independent Claims 17, 22, and 26. The liner oxide layer described by Zhou et al is not described in such a way as to provide a definitive conclusion that this layer is ever located over the gate structure and, if so located, that this layer remains, post etching of the spacers, located over the gate structure. Further, Zhou et al clearly shows layers 40 and 50 overlying the gate structure 20 in Fig. 1 and then shows no layers overlying the gate structure 20 in Fig. 2 after the spacer etching. Applicant believes that this observation, alone, makes a finding of rejection under 35 U.S.C. 102(e) due to anticipation by Zhou et al unsupportable. Zhou et al simply does

not appear to provide proof of anticipation of Applicant's claimed invention.

Therefore, Applicant respectfully requests that the rejection of independent Claims 17, 22, and 26 under 35 U.S.C. 102(e) be rescinded. Further, Claims 18, 21, 23, and 27 represent patentably distinct, further limitations of Claims 17, 22, and 26 and that, likewise, should not be rejected under 35 U.S.C. 102(e).

Reconsideration of Claims 17, 18, 21-23, 26, and 27 rejected under 35 U.S.C. 102(e) as being anticipated by Zhou et al 6,156,598 is requested based on the following remarks.

Applicants have reviewed the prior art made of record and not relied upon and have discussed their impact on the present invention above.

Allowance of all Claims is requested.

It is requested that should the Examiner not find that the Claims are now Allowable that the Examiner call the undersigned at 989-894-4392 to overcome any problems preventing allowance.

Respectfully submitted,

Douglas R Schnabel

Douglas R. Schnabel, Reg. No. 47,927